WHAT IS CLAIMED IS:

1. A method of manufacturing a semiconductor device comprising:

forming a pair of gate structures having opposed sidewalls on a semiconductor substrate;

forming a first spacer on the opposed sidewalls of the pair of gate structures;

forming a plurality of first contact pads on the substrate between the pair of gate structures, wherein adjacent first contact pads have opposing sidewalls, and wherein the height above the substrate of each first contact pad is less than the height above the substrate of the pair of gate structures;

forming a second spacer on at least some of the opposing sidewalls of the first contact pads; and

forming a second contact pad on at least some of the first contact pads.

2. The method of Claim 1, wherein the second spacers are further formed between the pair of gate structures and the first contact pads.

3. The method of Claim 2, wherein the height of each first contact pad above the substrate is between about 30 percent and about 60 percent of the height above the substrate of the pair of gate structures.

4. The method of Claim 1, wherein the height of portions of each second spacer above the substrate is between about 30 percent and about 60 percent of the height above the substrate of the pair of gate structures.

5. The method of Claim 2, wherein the first contact pads and the second contact pads comprise semiconductor materials formed using a selective epitaxial growth process.

6. The method of Claim 5, wherein the first contact pads comprise contact pads formed of silicon doped with impurities and/or silicon germanium doped with impurities.

7. The method of Claim 6, wherein the first contact pads are formed by introducing a dopant gas in-situ during the growth of the first contact pads.

8. The method of Claim 2, wherein the first contact pads are formed using an ion implantation process.

9. The method of Claim 1, wherein the second contact pads comprise contact pads formed of silicon doped with impurities or silicon germanium doped with impurities.

10. The method of Claim 5, wherein the second contact pads are formed by introducing a dopant gas in-situ during the growth of the second contact pads.

11. The method of Claim 5, wherein the second contact pads are formed using an ion implantation process.

12. The method of Claim 1, wherein the first spacer comprises a silicon oxide and/or silicon nitride film.

13. The method of Claim 1, wherein the first spacer has a thickness of from about 50Å to about 300Å.

14. The method of Claim 1, wherein the second spacer comprises a silicon oxide and/or a silicon nitride spacer.

15. The method of Claim 1, wherein the second spacer has a thickness of from about 50Å to about 100Å.

16. The method of Claim 1, wherein each first contact pad is formed to a predetermined height to prevent horizontal growth of the first contact pads forming an electrical short between one or more adjacent first contact pads.

17. The method of Claim 1, further comprising selectively forming a metal silicide layer on the second contact pads.

18. The method of Claim 17, wherein the metal silicide layer comprises cobalt silicide, titanium silicide and/or nickel silicide.

19. A method of manufacturing a semiconductor device comprising:

forming a plurality of cell gate structures and a plurality of peripheral gate structures on a semiconductor substrate having a cell area and a peripheral circuit area

in which a plurality of active regions are defined, wherein the cell gate structures have a first height above the substrate;

forming a first insulation film on the cell gate structures, on the peripheral gate structures and on the semiconductor substrate;

forming a second insulation film on the first insulation film that has an etching selectivity relative to the first insulation film;

selectively etching the second insulation film to leave the second insulation film on the peripheral circuit area only;

selectively etching the first insulation film to form a first spacer on at least one sidewall of each of the cell gate structures;

forming a plurality of first contact pads having a second height above the substrate on the active region between the cell gate structures, wherein the first height is greater than the second height;

forming a second contact pad on each of the first contact pads; and

forming a plurality of third contact pads on the active regions of the peripheral circuit area.

20. The method of Claim 19, further comprising forming a second spacer on at least some of the sidewalls of the first contact pads.

21. The method of Claim 20, further comprising forming the second spacers on sidewalls of the first spacers and on the second insulation film positioned on the peripheral gate structures.

22. The method of Claim 19, wherein the second height is between about 30 percent and about 60 percent of the first height.

23. The method of Claim 19, wherein the first contact pads and the second contact pads comprise semiconductor materials formed using a selective epitaxial growth process.

24. The method of Claim 19, wherein the first contact pads, the second contact pads and the third contact pads each comprise contact pads formed of silicon doped with impurities and/or silicon germanium doped with impurities.

25. The method of Claim 19, wherein one of the first insulation film and

the second insulation film comprises a silicon oxide film and the other of the first insulation film and the second insulation film comprises a silicon nitride film.

26. The method of Claim 19, wherein the first spacers have a thickness of from about 50Å to about 300Å.

27. The method of Claim 19, further comprising selectively forming metal silicide layers on the second contact pads and on the third contact pads.

28. The method of Claim 27, wherein the metal silicide layers comprise cobalt silicide, titanium silicide and/or nickel silicide.

29. The method of Claim 19, wherein each first contact pad is formed to a predetermined height to prevent horizontal growth of the first contact pads creating forming an electrical short between one or more adjacent first contact pads.

30. The method of Claim 21, wherein the forming the second spacers further comprises:

forming a third insulation film on the semiconductor substrate including the first contact pads formed thereon, wherein the third insulation film has a substantially same etching rate as the second insulation film;

anisotropically etching the third insulation film and the second insulation film on the peripheral circuit area in order to leave the third insulation film on the first spacers positioned on the first contact pads and on the second insulation film formed on the peripheral gate structures; and

removing the first insulation film from the peripheral circuit area.

31. The method of Claim 19, further comprising implanting impurities into the first contact pads and into the third contact pads after forming the second contact pads and the third contact pads.

32. The method of Claim 31, wherein implanting impurities further comprises:

selectively implanting n-type impurities into the first contact pads, into the second contact pads and into the third contact pads connected to source/drain regions of n-type MOS transistors; and

selectively implanting p-type impurities into the first contact pads, the second contact pads and the third contact pads connected to source/drain regions of p-type MOS transistors.

33. A semiconductor device comprising:

a plurality of gate structures on a semiconductor substrate in which a plurality of active regions are defined;

a first spacer on each sidewall of the gate structures;

a plurality of first contact pads on the substrate between adjacent gate structures, the first contact pads having heights lower than the heights of the gate structures;

a plurality of second spacers, wherein at least one second spacer is provided between adjacent ones of the first contact pads; and

a second contact pad on each of the first contact pads.

34. A semiconductor device comprising:

a substrate having a plurality of active regions in both a cell area and a peripheral circuit area;

a plurality of cell gate structures on the cell area of the substrate and a plurality of peripheral gate structures on the peripheral circuit area of the substrate, wherein the cell gate structures have a first height above the substrate;

a first spacer on at least some of the sidewalls of the cell gate structures;

a plurality of first semiconductor contact pads positioned between the cell gate structures on the active regions, the first contact pads having a second height that is less than the first height;

an insulation film pattern on the peripheral gate structures;

a second spacer on a sidewall of at least some of the first spacers, on a sidewall of at least some of the first semiconductor contact pads, and on a sidewall of the insulation film patterns;

a second semiconductor contact pad on each of the first semiconductor contact pads; and

a plurality of third semiconductor contact pads on the active regions of the peripheral circuit area.